UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/584,038	06/21/2006	Godefridus Adrianus Maria Hurkx	NL04 0842 US1	6992

24738 7590 03/12/2008

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
370 W. TRIMBLE ROAD MS 91/MG
SAN JOSE, CA 95131

EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
4146	

MAIL DATE	DELIVERY MODE
03/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/584,038	HURKX ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	4146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/21/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Specification

1. The abstract of the disclosure is objected to because it is included with the cover page of the corresponding PCT application. A separate abstract is requested with only the abstract on the page. Correction is required. See MPEP § 608.01(b).

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: A Nanostructure device Comprising a PN-Heterojunction.

3. The disclosure is objected to because of the following informalities:

a. Page 4, line 30 has a typo: "te" should read "the"

b. Page 7, lines 5 and 6 contain numbers in parentheses. It is unclear as to what they numbers are referring.

c. Page 8, line 8 has a typo: "Ohmcm" should read "Ohm-cm"

d. Page 9, line 18 has a typo: "not" should read "no"

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 3, 5, 6, and 9 – 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Majumdar et al. (US 2002/01755408 A1).

a. Regarding claim 1, Majumdar discloses **an electric device** (e.g. see figures 3 and 10, referred to as longitudinal heterostructure nanowire LOHN) comprising

a semiconductor body (p-body part of figure 10) comprising a group IV semiconductor material having a surface,

a nanostructure (n-body part of figure 10**) of a III-V semiconductor material** (e.g. paragraph [0099] discloses that the nanowire heterostructures can be made of semiconductor materials selected from groups III-V and II-IV),

characterized in that the nanostructure is a nanowire being positioned in direct contact with the surface and having a first conductivity

type (e.g. as seen in figure 10, the n-nanowire is in direct contact with the p-body),

the semiconductor body having a second conductivity type opposite to the first conductivity type (e.g. as seen in figure 10, they are of opposite conductivities: p-type and n-type),

the nanowire forming with the semiconductor body a pn-heterojunction (e.g. as seen in figure 10, and further illustrated in figure 16).

b. Regarding claim 2, Majumdar discloses **an electric device as claimed in Claim 1, as cited above, characterized in that the III-V material is a diffusion source of dopant atoms into the semiconductor body** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN, where the dopant concentrations of the two materials overlap and are diffuse into one another. Since the nanowire is made of III-V materials, its material is a source of dopant atoms).

c. Regarding claim 3, Majumdar discloses **an electric device as claimed in Claim 2, as cited above, characterized in that the diffusion source contains the group III atoms and/or the group V atoms from the III-V material** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN, where the base material concentrations of the two materials overlap

and are diffuse into one another. Since the nanowire is made of III-V materials, its material is a source of dopant atoms).

d. Regarding claim 5, Majumdar discloses **an electric device as claimed in Claim 2, as cited above, characterized in that the III-V material comprises an excess of the group III atoms and/or the group V atoms of the III-V material, which excess atoms form the dopant atoms in the semiconductor body** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN, where the excess base material and excess dopant material of the n-type nanowire overlaps with the base material and dopant material of the p-type semiconductor body, thus forming a dopant concentration in the semiconductor body).

e. Regarding claim 6, Majumdar **discloses a device according to claim 1, as cited above, characterized in that the nanowire is in epitaxial relationship with the semiconductor body and the materials have a mutual lattice mismatch** (e.g. paragraphs [0105] and [0106] discuss the heteroepitaxy in nanowires, and their growth, and discuss the lattice mismatch between adjacent material regions).

f. Regarding claim 9, Majumdar discloses **a device according to claim 1, as cited above, characterized in that the nanowire is a substantially single-**

crystal nanowire (e.g. paragraph [0008] discusses that the heterostructure nanowires made be formed from homostructures, which are substantially monocrystalline).

g. Regarding claim 10, Majumdar discloses **a device according to claim 1, as cited above, characterized in that a plurality of nanowires are arranged in an array** (e.g. see figure 25).

h. Regarding claim 11, Majumdar discloses **a method of forming a pn-heterojunction device** (e.g. see figures 3 and 10, referred to as longitudinal heterostructure nanowire LOHN), **the method comprising the steps of**

forming a nanostructure (n-body part of figure 10) **of a second semiconductor material on a surface of a semiconductor body** (p-body part of figure 10) of a first semiconductor material,

the first semiconductor material comprising at least one element from group IV of the periodic system and the second semiconductor material being a III-V material (e.g. paragraph [0099] discloses that the nanowire heterostructures can be made of semiconductor materials selected from groups III-V and II-IV),

characterized in that the nanostructure is a nanowire grown on the surface of the semiconductor body and receiving a first conductivity type

(e.g. as seen in figure 10, the first conductivity type is n-type, and grown using a vapor-liquid-solid (VLS) method discussed in paragraphs [0068] and [0089]),

the semiconductor body having a second conductivity type opposite to the first conductivity type (p-type, as seen in figure 10),

the nanowire forming with the semiconductor body a pn-heterojunction (e.g. as seen in figure 10, and further illustrated in figure 16).

i. Regarding claim 12, Majumdar discloses **a method as claimed in Claim 11, as cited above, characterized in that the nanowire of III-V semiconductor material is used as a diffusion source of dopant atoms into the semiconductor body** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN, where the dopant concentrations of the two materials overlap and are diffuse into one another. Since the nanowire is made of III-V materials, its material is a source of dopant atoms).

j. Regarding claim 13, Majumdar discloses **a method as claimed in Claim 12, as cited above, characterized in that group III atoms and/or the group V atoms from the III-V material are the dopant atoms** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN, where the base material concentrations of the two materials overlap and are diffuse into one another. Since the nanowire is made of III-V materials, its material is a source of dopant atoms).

k. Regarding claim 14, Majumdar discloses **a method as claimed in Claim 11, as cited above, characterized in that the nanowire is grown in epitaxial relationship with the semiconductor body** (e.g. paragraphs [0105] and [0106] discuss the heteroepitaxy in nanowires).

l. Regarding claim 15, Majumdar discloses **a method as claimed in Claim 14, as cited above, characterized in that the nanowire is grown according to the vapor-liquid-solid (VLS) growth method** (e.g. paragraphs [0068] and [0089] discuss the VLS method of growth for the nanowire heterostructures).

m. Regarding claim 16, Majumdar discloses **a method as claimed in 14, as cited above, characterized in that an excess of the group III atoms and/or the group V atoms are grown in the III-V semiconductor material, which excess atoms are diffused into the semiconductor body** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN, where the excess base material and excess dopant material of the n-type nanowire overlaps with the base material and dopant material of the p-type semiconductor body, thus forming a dopant concentration in the semiconductor body. Since the nanowire is made of III-V materials, its material is a source of excess atoms).

n. Regarding claim 17, Majumdar discloses a **method as claimed in claim 14**, as cited above, **characterized in that at least one element of the periodic system is incorporated in the III-V semiconductor material of the nanowire** (e.g. paragraph [0076] discloses that the nanowires may be doped with B, Ph, As, In, Al, and other elements), **which element is diffused into the group IV semiconductor material, forming an n-type or p-type dopant atom.** (Paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN, where the excess base material and excess dopant material of the n-type nanowire overlaps with the base material and dopant material of the p-type semiconductor body, thus forming a dopant concentration in the semiconductor body. Since the nanowire is made of III-V materials, along with dopants B, Ph, As, In, Al, and others, its base material and dopants are a source of excess atoms. The dopant atom forms either an n-type or p-type dopant, as discussed in paragraph [0076]).

o. Regarding claim 18, Majumdar discloses **a method as claimed in claim 11, as cited above, characterized in that the dopant atoms form a region in the semiconductor body in direct contact with the nanowire** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN of figure 10, where the dopant material concentrations of the two materials overlap and are diffuse into one another. Since the nanowire is made of III-V

materials with dopants, its material is a source of dopant atoms in the adjacent region).

p. Regarding claim 19, Majumdar discloses **a method as claimed in 11, as cited above, characterized in that the III-V semiconductor material of the nanowire is heated above 600 °C** (e.g. the wire is surrounded by a sheath, as seen in figure 5, and then heated, as disclosed in paragraphs [0111] and [0112]).

q. Regarding claim 20, Majumdar discloses **a method as claimed in Claim 19, as cited above, characterized in that the nanowire is embedded in a dielectric before heating** (e.g. paragraph [0112] states that, prior to heating, the nanowire may be embedded in a sheath made of SiO_2, which is a dielectric).

r. Regarding claim 21, Majumdar discloses **a method as claimed in claim 12, characterized in that the nanowire is selectively removed after being used as diffusion source** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN, where the dopant concentrations of the two materials overlap and are diffuse into one another. Since the nanowire is made of III-V materials, its material is a source of dopant atoms diffused into the body. Paragraph [0112] discussing removing the nanowire from an surrounding sheath, by melting it away)

6. Claims 4 and 7 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Majumdar.

a. Regarding claim 4, Majumdar discloses **an electric device as claimed in claim 1, characterized in that there is a region in the semiconductor body in direct contact with the nanowire, which has the same conductivity type as the nanowire** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN of figure 10, where the dopant material concentrations of the two materials overlap and are diffuse into one another. Since the nanowire is made of III-V materials with dopants, its material is a source of dopant atoms in the adjacent region. Because the structure of the invention of Majumdar is the same as that claimed by the applicant, the properties of the claimed invention are obvious to the device of the prior art. Hence, there is a region of the semiconductor body that has the same conductivity of the n-type nanowire, especially where the transition region comprises a large percentage of n-type nanowire material and a small portion of p-type semiconductor body).

b. Regarding claim 7, Majumdar discloses **a device according to claim 2, characterized in that the resistance between the nanowire and the semiconductor body is below 10^{-5} Ohm cm^2** (e.g. paragraph [0084] discloses a transitional region between the adjacent materials in a LOHN of figure 10, where the dopant material concentrations of the two materials overlap and are diffuse

into one another. Since the nanowire is made of III-V materials with dopants, its material is a source of dopant atoms in the adjacent region. Because the structure of the invention of Majumdar is the same as that claimed by the applicant, the properties the claimed invention are obvious to the device of the prior art. There is a region of the semiconductor body that has the same conductivity of the n-type nanowire, especially where the transition region comprises a large percentage of n-type nanowire material and a small portion of p-type semiconductor body. Hence, one expects in this region to have a resistivity less than 10^{-5} Ohm cm^2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Majumdar in view of Chen et al. (US 2003/0180989 A1). Majumdar discloses a device according to claim 1, characterized in that a lattice mismatch exists between the semiconductor body and the nanowire (e.g. paragraphs [0105] and [0106] discuss the heteroepitaxy in nanowires and their growth, and discuss the lattice mismatch between adjacent material regions). Majumdar is silent with respect to the lattice mismatch being smaller than

10%. Chen discloses a device comprising a nanowire on a semiconductor region with a lattice mismatch of less than 4% (paragraphs [0010] and [0011]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to adjust the lattice mismatch of the device of Majumdar such that it is lower than 10%, as suggested by Chen. One would be motivated to construct a device with such a small lattice mismatch in order to promote growth of the crystalline nanowire, as discussed by Chen (paragraph [0010]).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Lieber et al. (US 2002/0130311 A1) discloses Doped Elongated Semiconductors, Growing Such Semiconductors, Devises Including Such Semiconductors, and Fabricating Such Devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (8am - 5pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marvin Lateef can be reached on (571) 272-5026. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 4146
February 29, 2008

/Marvin M. Lateef/
Supervisory Patent Examiner, Art Unit 4146